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10/712,640	11/12/2003	Rameshkumar G. Illikkal	42P16966	8973

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EXAMINER	
MERED, HABTE	

ART UNIT	PAPER NUMBER
2616	

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12/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/712,640	ILLIKKAL, RAMESHKUMAR G.	
	Examiner	Art Unit	
	Habte Mered	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,13-18,20-22 and 24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13-18,20-22 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 10/01/2007 has been entered and fully considered.

2. Claims 1-10, 13-18, 20-22, and 24-25 are pending. Claims 1, 8, 14, and 21 are the base independent claims. Claims 11, 12, 19, and 23 are cancelled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A) Claims 1, 7-9, 14-17, 20-22, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Banerjee (US 6, 820, 127 B2) in view of Brustoloni et al (US 6, 625, 149 B1), hereinafter referred to as Brustoloni and Ganfield (US Pub. No. 20040218631).

Banerjee teaches a method and system for establishing cache for storing Protocol Control Block.

1. Regarding **claims 1 and 14**, Banerjee teaches a method and an article of manufacture with a machine accessible medium that includes a content when accessed by a machine causes the machine to execute the steps comprising: receiving a packet at a network device **(Figure 5, step 502 and Column 7:25-30)**; pre-fetching a protocol control block (PCB) associated with the packet into a cache of a selected processing unit **(Figure 5, step 522 and Column 8:1-6 and also Figure 4, step 414 – any of the processors 202 or 204 in figure 2 can be the selected processors and each of**

them can have their own PCB cache as illustrated in Column 5:25-32); and retrieving the PCB from the cache of the selected processing unit when the selected processing unit is ready to process the packet **(Figure 5, steps 504, 508, 512 and 513 and Column 7:30-42).**

Banerjee, however, fails to expressly disclose queuing the received packet for processing. However, Banerjee does in fact teach that the socket process has a receive and send buffers in Column 2:10-15 and in Column 3:33-38 that a priority is assigned to each process which strongly implies the presence of a queuing system in Banerjee:

Brustoloni teaches a receiver capable of handling packets based on different protocols.

Brustoloni teaches queuing the received packets for processing. **(See Figure 3, element 80)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Banerjee's method and article to incorporate the step of queuing the received packets for processing. The motivations for queuing the received packets is to prevent the overflow of the socket send buffers.

Banerjee fails to disclose a method and article, further comprising pre-fetching a header associated with the packet into the cache of the selected processing unit.

Ganfield discloses a method and apparatus for implementing packet work area access and buffer sharing.

Ganfield discloses a method, and article, further comprising pre-fetching a header associated with the packet in the cache of the selected processing unit. **(Figure 5B, elements 530 and 526 and Paragraphs 32 and 38)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Banerjee's method and article by incorporating a step for comprising pre-fetching a header associated with the packet in cache. The motivation to save the header associated with the packet into the cache memory is to minimize processor time by minimizing latency caused by unnecessary repeated access to memory as implied by Ganfield in Paragraphs 38 and 39.

2. Regarding **claim 8**, Banerjee discloses an apparatus **(See Figure 2)** comprising: a receive unit to receive a packet **(Figure 2, elements 218 and 220)**; a pre-fetch unit coupled to the receive unit to pre-fetch a protocol control block (PCB) associated with the packet into a cache **(Figure 2, elements 208 and 208A)** of a processing unit **(any of the processors 202 or 204 in figure 2 can be the selected processors and each of them can have their own PCB cache as illustrated in Column 5:25-32)**; and the processing unit coupled to the pre-fetch Unit to retrieve the PCB from the cache and process the packet **(Figure 2, elements 202 and 204).**

Banerjee, however, fails to expressly disclose a pre-fetch unit coupled to the receive unit queuing the received packet for processing.

Brustoloni teaches a pre-fetch unit **(Figure 3, element 50 and see also Column5: 38-45)** coupled to the receive unit **(Figure 3, element 82)** queuing the received packet for processing **(Figure 3, element 80 and Column 6:55-65)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Banerjee's apparatus by incorporating a pre-fetch unit coupled to the receive unit queuing the received packet for processing. The motivations for queuing the received packets is to prevent the overflow of the socket send buffers as stated in Brustoloni Column 6:66-67.

Banerjee fails to disclose an apparatus, further comprising a pre-fetching unit that pre-fetches and retrieves a header associated with the packet into and from the cache of the processing unit respectively.

Ganfield discloses an apparatus, further comprising a pre-fetching unit **(Figure 1, element 106 and see paragraph 39)** that pre-fetches and retrieves a header associated with the packet into the cache of the processing unit respectively. **(Figure 5B, elements 530 and 526 and Paragraphs 32, 38 and 39)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Banerjee's apparatus by incorporating an apparatus further comprising a pre-fetching unit that pre-fetches and retrieves a header associated with the packet into the cache of the processing unit respectively. The motivation to save the header associated with the packet into the cache memory is to minimize processor time by minimizing latency caused by unnecessary repeated access to memory as implied by Ganfield in Paragraphs 38 and 39.

3. Regarding **claim 21**, Banerjee discloses a system comprising: a receive unit to receive a packet **(Figure 2, elements 218, 220)**; a memory coupled to the receive unit to store the received packet **(Figure 2, element 209)**; a memory controller coupled to

the memory to manage the memory **(Figure 2, element 208)**; a pre-fetch unit coupled to the receive unit to pre-fetch a protocol control block (PCB) associated with the packet into a cache**(Figure 2, element 208A)**; and a processing unit to retrieve the PCB from the cache and process the packet **(Figure 2, elements 202 and 204)**.

Banerjee, however, fails to expressly disclose a pre-fetch unit coupled to the receive unit queuing the received packet for processing.

Brustoloni teaches a pre-fetch unit **(Figure 3, element 50 and see also Column5: 38-45)** coupled to the receive unit **(Figure 3, element 82)** queuing the received packet for processing **(Figure 3, element 80 and Column 6:55-65)**.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Banerjee's system by incorporating a pre-fetch unit coupled to the receive unit queuing the received packet for processing. The motivations for queuing the received packets is to prevent the overflow of the socket send buffers as stated in Brustoloni Column 6:66-67.

Banerjee fails to disclose a system, further comprising a pre-fetching unit that pre-fetches a header associated with the packet into a cache of a processor and a processing unit to retrieve the PCB from the cache of the processor.

Ganfield discloses disclose a system, further comprising a pre-fetching unit **(Figure 1, element 106 and see paragraph 39)** that pre-fetches a header associated with the packet into a cache of a processor and a processing unit to retrieve the PCB from the cache of the processor. **(Figure 5B, elements 530 and 526 and Paragraphs 32, 38 and 39)**

. It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Banerjee's system by incorporating an apparatus further comprising a pre-fetching unit that pre-fetches a header associated with the packet into a cache of a processor and a processing unit to retrieve the PCB from the cache of the processor. The motivation to save the header associated with the packet into the cache memory is to minimize processor time by minimizing latency caused by unnecessary repeated access to memory as implied by Ganfield in Paragraphs 38 and 39.

4. Regarding **claims 7 and 17**, Banerjee discloses a method and article of manufacture, further comprising processing the packet. **(Column 2:25-28 and Figure 7, Blocks 704 and 718)**

5. Regarding **claims 9 and 22,** the combination of Banerjee, Ganfield, and Brustoloni discloses an apparatus and system where the receive unit is a network interface card. **(Banerjee Column 2:30 and Figure 7, Block 702 and also Brustoloni Column 4:25-26)**

6. Regarding **claim 15**, the combination of Banerjee, Ganfield and Brustoloni disclose an article of manufacture, wherein the machine-accessible medium further includes content that causes the machine to pre-fetch the header associated with the packet in the cache. **(Ganfield Figure 5B, elements 530 and 526 and Paragraphs 32, 38 and 39)**

7. Regarding **claims 16 and 24,** the combination of Banerjee, Ganfield and Brustoloni discloses an article of manufacture and system, further comprising retrieving

the packet header from the cache when the processing unit is ready to process the packet. **(Ganfield Paragraph 39)**

8. Regarding **claim 20**, Banerjee discloses an article of manufacture, further comprising storing the packet in a memory coupled to the processing unit. **(Column 6:2-5)**

B) Claims 2-6, 10, 13, 18 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Banerjee in view of Brustoloni and Ganfield as applied to claims 1, 8, 14 and 25 above, and further in view of Kaniyar et al (US 7, 219, 121), Hereinafter referred to as Kaniyar.

1. Regarding **claim 2**, the combination of Banerjee, Brustoloni, and Ganfield fail to disclose a method further comprising checking the destination of the interrupt and disabling interrupts from a network interface.

Kaniyar teaches symmetrical multiprocessing in multiprocessor systems.

Kaniyar discloses a method further comprising checking the destination of the interrupt and disabling interrupts from a network interface. **(See Figure 4, steps 408, 410, 412 and the abstract and Column 1:44-67 and Column 2:34-67 and Column 3:1-30 and Column 6:46-67 and Column 8:15-67)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Banerjee's, Brustoloni's, and Ganfield's method by incorporating a step further comprising checking the destination of the interrupt and disabling interrupts from a network interface. The motivation to select the destination of an interrupt is to ensure the same processor is always selected in

order to ensure that Input/Output tasks associated with a particular connection are processed by the same processor as indicated by Kaniyar in Column 2:40-45.

2. Regarding **claim 3**, the combination of Banerjee, Brustoloni, Ganfield, and Kaniyar teach a method of further comprising retrieving the packet header from the cache associated with the selected processor unit when the processing unit is ready to process the packet. **(See Ganfield Paragraph 39 and Kaniyar Figure 4, steps 408, 410, 412 and column 18:15-67)**

3. Regarding **claims 4, 13, 18, and 25**, the combination of Banerjee, Ganfield, and Brustoloni discloses a method, an apparatus, an article of manufacture, and system, further comprising sending an interrupt to notify the processing unit of the receipt of the packet. **(See Banerjee Column 2:29-34 and Figure 7, step 704 and Brustoloni Column 5:33-37 and Figure 3, element 40 (i.e. interrupt unit))**

However, the combination of Banerjee, Ganfield, and Brustoloni fail to expressly disclose a method, further comprising sending an interrupt to notify the selected processing unit of the receipt of the packet.

Kaniyar discloses a method, further comprising sending an interrupt to notify the selected processing unit of the receipt of the packet. **(See Figure 4, steps 408, 410, 412 and the abstract and Column 1:44-67 and Column 2:34-67 and Column 3:1-30 and Column 6:46-67 and Column 8:15-67)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Banerjee's, Brustoloni's, and Ganfield's method, apparatus, article of manufacture, and system by incorporating a

step further comprising sending an interrupt to notify the selected processing unit of the receipt of the packet. The motivation to select the destination of an interrupt is to ensure the same processor is always selected in order to ensure that Input/Output tasks associated with a particular connection are processed by the same processor as indicated by Kaniyar in Column 2:40-45.

4. Regarding **claim 5**, the combination of Banerjee, Brustoloni, Ganfield, and Kaniyar teach a method wherein the interrupt is software. **(See Kaniyar Column 5:63-67 and Column 6:46-52 and Kaniyar Deferred Procedure Call (DPC) is a software interrupt as a procedure call is simply a function call in Microsoft Operating software and Kaniyar has indicated that DPC is well known in the art and needs no further explanation. However if Applicant wants to prove DPC is indeed a software interrupt beyond a shadow of doubt then please refer to Gaur et al (US Pub. No. 20020144004) or Ballantyne (US 6990669))**

5. Regarding **claim 6**, the combination of Banerjee, Brustoloni, Ganfield, and Kaniyar discloses a method, further comprising storing the packet in a memory coupled to the processing unit. **(Banerjee Column 6:2-5)**

6. Regarding **claim 10**, the combination of Banerjee, Brustoloni, and Ganfield fail to disclose an apparatus further comprising an interrupt service unit to check the destination of the interrupt, disable further interrupts from the network interface card, initiate a software interrupt, and queue the packet for processing.

Kaniyar discloses an apparatus further comprising an interrupt service unit **(Figure 3, element 327 and Column 5:64-67 and Column 6:44-67)** to check the destination of

the interrupt, disable further interrupts from the network interface card, initiate a software interrupt, and queue the packet for processing. **(See Figure 4, steps 408, 410, 412 and the abstract and Column 1:44-67 and Column 2:34-67 and Column 3:1-30 and Column 6:46-67 and Column 8:15-67)**

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Banerjee's, Brustoloni's, and Ganfield's apparatus by incorporating a step further comprising an interrupt service unit to check the destination of the interrupt, disable further interrupts from the network interface card, initiate a software interrupt, and queue the packet for processing. The motivation to select the destination of an interrupt is to ensure the same processor is always selected in order to ensure that Input/Output tasks associated with a particular connection are processed by the same processor as indicated by Kaniyar in Column 2:40-45.

Response to Arguments

1. Applicant's arguments filed 10/1/2007 have been fully considered but they are not persuasive.

2. In the Remarks, on page 6, in the last paragraph, Applicant argues with respect to amended claim 1, the deficiency of the combination of Banerjee and Brustoloni in addressing the limitation requiring "pre-fetching a header associated with the packet into the cache of the selected processing unit" cannot be remedied by Ganfield. The sole reason provided by the Applicant in disqualifying Ganfield as a prior art is that the cache 530 is coupled to the data flow processor 106 and the control processor 104 and fails to be a cache of the selected processor.

Examiner respectfully disagrees with Applicant's conclusions. First, just simply focusing on the claim language, claim 1 is only requiring that pre-fetching a header associated with a packet into the cache of the selected processor. The claim language does not "exclude sharing a cache memory between different processors". Given this fact Ganfield is still applicable as a prior art. Even if the claim language in the future is amended to exclude sharing of cache between processors, the primary reference, Banerjee, in no uncertain term teaches that cache memory can be shared between processors or can be unique to a processor as illustrated in Banerjee's Column 5:27-32. Examiner would like to emphasize the reason why Brustoloni was introduced is simply to teach header associated with an incoming or received packet can be placed in a cache memory for speedy retrieval and the fact that the cache is shared or not is irrelevant as it is already taught by the primary reference (Banerjee). Hence, the 103 rejections of all independent claims based on the previously cited prior arts are maintained.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Habte Mered whose telephone number is 571 272 6046. The examiner can normally be reached on Monday to Friday 9:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris H. To can be reached on 571 272 7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system.

Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HM
12-7-2007

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